Serial No.: 10/051,062
Docket No.: NEG-241
KATO.021

AMENDMENTS TO THE CLAIMS:

1. (Currently amended) A system for enabling facilitated analysis of malfunctions in a computer device, said system comprising:

a processor unit;

a PCI bus;

a plurality of PCI devices connected to said processor unit by said PCI bus, each PCI device, when operating as a PCI target device, activating a corresponding target operating signal; and

a PCI bus monitor circuit for monitoring a target address of a command from said processor unit to be executed on said PCI bus and monitoring the target operating signals from said plurality of PCI devices, said PCI bus monitor circuit sending an error report signal to said processor unit when plural PCI target devices respond to the command in one PCI cycle.

2. (Previously presented) The system as defined in claim 1, wherein said PCI bus monitor circuit comprises:

an address storage circuit for monitoring the operation of said PCI bus at the time of booting said computer device to store base address values and size values of said plurality of PCI devices in association with the target operating signals;

an address latch circuit for storing temporarily the target address;

a target device selection circuit for specifying the PCI target device based on the base address values and size values of said plurality of PCI devices stored in said address storage

circuit and on the target address temporarily stored in said address latch circuit;

a target comparator circuit for comparing a result of said target device selection circuit and states of said target operating signals and for detecting that plural PCI target devices have responded in one PCI cycle; and

an error status circuit for storing the result of said target device selection circuit and plural target operating signals from said target comparator circuit to report to said processor unit that plural PCI target devices have responded in one PCI cycle by way of the error report signal.

3. (Previously presented) The system as defined in claim 1, wherein said PCI bus monitor circuit comprises:

an address storage circuit, in which base address values and size values of said plurality of PCI devices in association with the target operation signals are stored by the processor unit at the time of booting said computer device;

an address latch circuit for storing temporarily the target address;

a target device selection circuit for specifying the PCI target device based on the base address values and size values of said plurality of PCI devices stored in said address storage circuit and on the target address temporarily stored in said address latch circuit;

a target comparator circuit for comparing a result of the target device selection circuit and states of said target operating signals and for detecting that plural PCI target devices have responded in one PCI cycle; and

an error status circuit for storing the result of said target device selection circuit and

plural target operating signals from said target comparator circuit to report to said processor unit that plural PCI target devices have responded in one PCI cycle by way of the error report signal.

4. (Currently amended) A system for enabling facilitated analysis of malfunctions in a computer device, said system comprising:

a processor unit;

a PCI bus;

a plurality of PCI devices connected to said processor unit by said PCI bus, each PCI device, when operating as a PCI target device, activating a corresponding target operating signal; and

a PCI bus monitor circuit for monitoring a target address of a command from said processor unit to be executed on said PCI bus and monitoring the target operating signals from said plurality of PCI devices, said PCI bus monitor circuit including a unit for resetting said PCI bus when plural PCI target devices respond to the command in one PCI cycle.

5. (Previously presented) The system as defined in claim 4, wherein said PCI bus monitor circuit comprises:

an address storage circuit for monitoring the operation of said PCI bus at the time of booting said computer device to store base address values and size values of said plurality of PCI devices in association with the target operating signals;

an address latch circuit for storing temporarily the target address;

a target device selection circuit for specifying the PCI target device based on the base address values and size values of said plurality of PCI devices stored in said address storage circuit and on the target address temporarily stored in said address latch circuit;

a target comparator circuit for comparing a result of said target device selection circuit and states of said target operating signals and for detecting that plural PCI target devices have responded in one PCI cycle;

an error status circuit for storing the result of said target device selection circuit and plural target operating signals from said target comparator circuit; and

a PCI reset generating circuit for executing a reset operation of said PCI bus, with contents of said error status circuit being held by the PCI reset generating circuit to reset all of the PCI devices connected to said PCI bus.

6. (Previously presented) The system as defined in claim 4, wherein said PCI bus monitor circuit comprises:

an address storage circuit, in which base address values and size values of said plurality of PCI devices in association with the target operation signals are stored by the processor unit at the time of booting said computer device;

an address latch circuit for storing temporarily the target address;

a target device selection circuit for specifying the PCI target device based on the base address values and size values of said plurality of PCI devices stored in said address storage circuit and on the target address temporarily stored in said address latch circuit;

a target comparator circuit for comparing a result of the target device selection circuit

and states of said target operating signals and for detecting that plural PCI target devices have responded in one PCI cycle;

an error status circuit for storing the result of said target device selection circuit and plural target operating signals from said target comparator circuit; and

a PCI reset generating circuit for executing a reset operation of said PCI bus, with contents of said error status circuit being held by the PCI reset generating circuit to reset all of the PCI devices connected to said PCI bus.

7. (Previously presented) A system for enabling facilitated analysis of malfunctions in a computer device, said system comprising:

a PCI bus;

a processor unit connected to said PCI bus, said processor unit activating a corresponding target operating signal when operating as a PCI target device;

a plurality of PCI devices connected to said PCI bus, each of said PCI devices, when operating as a PCI target device, activating a corresponding target operating signal; and

a PCI bus monitor circuit for monitoring a target address of a command from said processor unit to be executed on said PCI bus and monitoring the target operating signals from said processor unit and from said plurality of PCI devices, said PCI bus monitor circuit sending an error report signal to said processor unit when plural PCI target devices have responded to the command in one PCI cycle.

8. (Previously presented) The system as defined in claim 7, wherein said PCI bus monitor

circuit comprises:

an address storage circuit for monitoring the operation of said PCI bus at the time of booting said computer device to store base address values and size values of said plurality of PCI devices in association with the target operating signals;

an address latch circuit for storing temporarily the target address;

a target device selection circuit for specifying the PCI target device based on the base address values and size values of said plurality of PCI devices stored in said address storage circuit and on the target address temporarily stored in said address latch circuit;

a target comparator circuit for comparing a result of said target device selection circuit and states of said target operating signals and for detecting that plural PCI target devices have responded in one PCI cycle; and

an error status circuit for storing the result of said target device selection circuit and plural target operating signals from said target comparator circuit to report to said processor unit that plural PCI target devices have responded in one PCI cycle by way of the error report signal.

9. (Previously presented) The system as defined in claim 7, wherein said PCI bus monitor circuit comprises:

an address storage circuit, in which base address values and size values of said plurality of PCI devices in association with the target operation signals are stored by the processor unit at the time of booting said computer device;

an address latch circuit for storing temporarily the target address;

a target device selection circuit for specifying the PCI target device based on the base address values and size values of said plurality of PCI devices stored in said address storage circuit and on the target address temporarily stored in said address latch circuit;

a target comparator circuit for comparing the result of said target device selection circuit and states of said target operating signals and for detecting that plural PCI target devices have responded in one PCI cycle; and

an error status circuit for storing the result of said target device selection circuit and plural target operating signals to report to said processor unit that plural PCI target devices have responded in one PCI cycle by way of the error report signal.

10. (Currently amended) A system for enabling facilitated analysis of malfunctions in a computer device, said system comprising:

a PCI bus;

a processor unit connected to said PCI bus, said processor unit activating a corresponding target operating signal when operating as a PCI target device;

a plurality of PCI devices connected to said PCI bus, each of said PCI devices, when operating as a PCI target device, activating a corresponding target operating signal; and

a PCI bus monitor circuit for monitoring a target address of a command from said processor unit to be executed on said PCI bus and monitoring the target operating signals from said plurality of PCI devices, said PCI bus monitor circuit including a unit for resetting said PCI bus when plural PCI target devices respond to the command in one PCI cycle.

11. (Previously presented) The system as defined in claim 10, wherein said PCI bus monitor circuit comprises:

an address storage circuit for monitoring the operation of said PCI bus at the time of booting said computer device to store base address values and size values of said plurality of PCI devices in association with the target operating signals;

an address latch circuit for storing temporarily the target address;

a target device selection circuit for specifying the PCI target device based on the base address values and size values of said processor unit and said plurality of PCI devices stored in said address storage circuit and on the target address temporarily stored in said address latch circuit;

a target comparator circuit for comparing a result of said target device selection circuit and states of said target operating signals and for detecting that plural PCI target devices have responded in one PCI cycle;

an error status circuit for storing the result of said target device selection circuit and plural target operating signals from said target comparator circuit; and

a PCI reset generating circuit for executing a reset operation of said PCI bus, with contents of said error status circuit being held by the PCI reset generating circuit to reset all of the PCI devices connected to said PCI bus.

12. (Previously presented) The system as defined in claim 10, wherein said PCI bus monitor circuit comprises:

an address storage circuit, in which base address values and size values of said

plurality of PCI devices in association with the target operation signals are stored by the processor unit at the time of booting said computer device;

an address latch circuit for storing temporarily the target address;

a target device selection circuit for specifying the PCI target device based on the base address values and size values of said processor unit and said plurality of PCI devices stored in said address storage circuit and on the target address temporarily stored in said address latch circuit;

a target comparator circuit for comparing the result of the target device selection circuit and states of said target operating signals and for detecting that plural PCI target devices have responded in one PCI cycle;

an error status circuit for storing the result of said target device selection circuit and plural target operating signals from said target comparator circuit; and

a PCI reset generating circuit for executing a reset operation of said PCI bus, with contents of said error status circuit held by the PCI reset generating circuit to reset all of the PCI devices connected to said PCI bus.

13. (Previously presented) The system as defined in claim 7, wherein:

said processor unit comprises a micro-processor, a host bridge and a memory, and

said target operating signal is sent from said host bridge to said PCI bus monitor circuit.

14. (Previously presented) The system as defined in claim 10, wherein:

said processor unit comprises a micro-processor, a host bridge and a memory, and

said target operating signal is sent from said host bridge to said PCI bus monitor circuit.

15. (Currently amended) A method of facilitated analysis of malfunctions in a computer device which includes a processor unit, a PCI bus, and a plurality of PCI devices connected to the processor unit by the PCI bus, the method comprising:

each PCI device, when operating as a PCI target device, activating a corresponding target operating signal,

monitoring a target address of a command from said processor unit to be executed on the PCI bus;

monitoring the target operating signals from the plurality of PCI devices, and

sending an error report signal to the processor unit when plural PCI target devices respond to the command in one PCI cycle.

16. (Previously presented) The method as defined in claim 15, wherein monitoring the target operating signals comprises:

specifying the PCI target device based on stored base address values and size values of the plurality of PCI devices and on a stored target address; and

comparing the specified PCI target device and states of the target operating signals.

17. (Previously presented) The method as defined in claim 16, wherein monitoring the target

operating signals further comprises:

storing base address values and size values of the plurality of PCI devices in association with the target operating signals; and

storing the target address.

18. (Previously presented) The method as defined in claim 16, wherein monitoring the target operating signals further comprises:

detecting that plural PCI target devices have responded in one PCI cycle; and

reporting to the processor unit that plural PCI target devices have responded for one PCI cycle by way of the error report signal.

19. (Currently amended) A method of facilitated analysis of malfunctions in a computer device which includes a processor unit, a PCI bus, and a plurality of PCI devices connected to the processor unit by the PCI bus, the method comprising:

at each PCI device, when operating as a PCI target device, activating a corresponding target operating signal;

monitoring a target address of a command from said processor unit to be executed on the PCI bus;

monitoring the target operating signals from the plurality of PCI devices; and

resetting the PCI bus when plural PCI target devices respond to the command in one PCI cycle.

20. (Previously presented) The method as defined in claim 19, wherein monitoring the target address comprises:

specifying the PCI target device based on stored base address values and size values of the plurality of PCI devices and on a stored target address; and

comparing the specified PCI target device and states of the target operating signals.

21. (Previously presented). The method as defined in claim 20, wherein monitoring the target address further comprises:

storing base address values and size values of the plurality of PCI devices in association with the target operating signals; and

storing the target address.

22. (Previously presented) The method as defined in claim 20, wherein monitoring the target address further comprises:

detecting that plural PCI target devices have responded in one PCI cycle; and

resetting the PCI bus to reset all of the PCI devices connected to the PCI bus.

23. (Currently amended) A method of facilitated analysis of malfunctions in a computer device which includes a processor unit, a PCI bus, and a plurality of PCI devices connected to said processor unit by the PCI bus, the method comprising:

activating a corresponding target operating signal when the processor unit is operating as a PCI target device;

activating, by each PCI device when operating as a PCI target device, a corresponding target operating signal; and

monitoring a target address of a command from the processor unit to be executed on the PCI bus;

monitoring the target operating signals from the processor unit and from the plurality of PCI devices; and

sending an error report signal to the processor unit when plural PCI target devices have responded to the command for one PCI cycle.

24. (Previously presented) The system as defined in claim 23, wherein monitoring the target operating signals comprises:

specifying the PCI target device based on stored base address values and size values of the plurality of PCI devices and on a stored target address; and

comparing the specified PCI target device and states of the target operating signals.

25. (Previously presented) The system as defined in claim 24, wherein monitoring the target operating signals further comprises:

storing base address values and size values of the plurality of PCI devices in association with the target operating signals; and

storing the target address.

26. (Previously presented) The method as defined in claim 24, wherein monitoring the

target address further comprises:

detecting that plural PCI target devices have responded for one PCI cycle; and

reporting to the processor unit that plural PCI target devices have responded for one PCI cycle by way of the error report signal.

27. (Currently amended) A method of facilitated analysis of malfunctions in a computer device which includes a processor unit, a PCI bus, and a plurality of PCI devices connected to said processor unit by the PCI bus, the method comprising:

activating a corresponding target operating signal when the processor unit is operating as a PCI target device;

activating, by each PCI device when operating as a PCI target device, a corresponding target operating signal; and

monitoring a target address of a command from the processor unit to be executed on the PCI bus;

monitoring the target operating signals from the plurality of PCI devices; and

resetting the PCI bus when plural PCI target devices respond to the command in one PCI cycle.

28. (Previously presented) The system as defined in claim 27, wherein monitoring the target address comprises:

specifying the PCI target device based on stored base address values and size values of the processor unit and the plurality of PCI devices and on a stored target address; and

comparing the specified PCI target device and states of the target operating signals.

29. (Previously presented) The system as defined in claim 28, wherein monitoring the target address further comprises:

storing base address values and size values of the plurality of PCI devices in association with the target operating signals; and

storing the target address.

30. (Previously presented). The method as defined in claim 28, wherein monitoring the target address further comprises:

detecting that plural PCI target devices have responded in one PCI cycle; and

resetting the PCI bus to reset all of the PCI devices connected to the PCI bus.

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RECORD OF PERSONAL INTERVIEW

The courtesy of Examiner Scott T. Baderman in extending a personal interview with the undersigned attorney is acknowledged with appreciation. During the interview, Chen Patent No. 5,544,332, applicant's invention, and claim 1 as amended above were discussed. Examiner Baderman stated that the amendments appear to overcome the present rejection. Examiner Baderman also commented that the application is under final rejection.